SYSTEM AND METHOD FOR SYSTEM AND METHOD FOR TESTING AN EMBEDDED MICROPROCESSOR SYSTEM CONTAINING PHYSICAL AND/OR SIMULATED HARDWARE

Abstract of the Disclosure

A system for testing an embedded system containing a target processor executing a target program and target hardware that may be partially physical and partially simulated. A target monitor determines when the target processor is attempting to access the simulated hardware. This determination is made by monitoring the address bus of the microprocessor to detect an address in the address space of the simulated hardware. An attempt to access the simulated hardware may also be detected by detecting the lack of an acknowledge signal from the physical hardware within a predetermined period after the target processor attempts to access the target hardware. In the event of an access to the simulated hardware, a bus capture circuit captures output signals on the bus connections of the target processor and converts the output signals to output data. The output data is then coupled through a communications interface to a hardware simulator. The hardware simulator processes the data in the same manner that the physical hardware would respond to signals corresponding to the output data. The hardware simulator may also generate data that are converted to corresponding input signals and applied to respective bus connections of the target processor by a bus driver circuit. During the time that output data is being processed by the hardware simulator, execution of the target program by the target processor is suspended, although the target processor may continue to service interrupts.